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Engineering the Interfaces of ITO@Cu_2S Nanowire Arrays toward Efficient and Stable Counter Electrodes for Quantum-Dot-Sensitized Solar Cells

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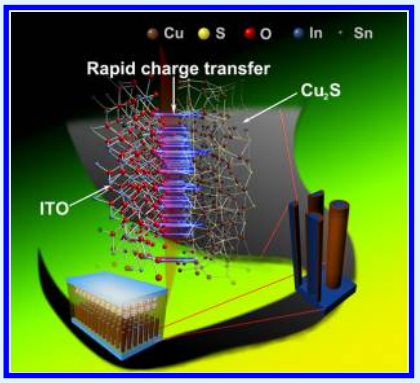
Supporting Information

ABSTRACT: Among the issues that restrict the power conversion efficiency (PCE) of quantum-dot-sensitized solar cells (QDSSCs), insufficient catalytic activity and stability of counter electrodes (CEs) are critical but challenging ones. The state-of-the-art Cu/Cu_2S CEs still suffer from mechanical instability and uncertainty due to the reaction of copper and electrolyte. Herein, ITO@Cu_2S core−shell nanowire arrays were developed to fabricate CEs for QDSSCs, which have no such issues in Cu/Cu_2S CEs. These nanowire arrays exhibited small charge transfer resistance and sheet resistance, and provided more active catalytic sites and easy accessibility for electrolyte due to the three-dimensional structure upon use as CEs. More interestingly, it was found that the interface of ITO/Cu_2S significantly affected the performance of ITO@Cu_2S nanowire array CEs. By varying synthetic methods, a series of ITO@Cu_2S nanowire arrays were prepared to investigate the influence of ITO/Cu_2S interface on their performance. The results showed that ITO@Cu_2S nanowire array CEs with a continuous Cu_2S nanocrystal shell fabricated via an improved cation exchange route exhibited excellent and thickness-dependent performance. The PCE of corresponding QDSSCs increased by 11.6 and 16.5% compared to that with the discrete Cu_2S nanocrystal and the classic Cu/Cu_2S CE, respectively, indicating its promising potential as a new type of CE for QDSSCs.



KEYWORDS: *nanowires, quantum dots, solar cells, interface, counter electrodes*

INTRODUCTION

The third generation solar cell requires higher power conversion efficiency (PCE) and lower production cost compared to the state-of-the-art photovoltaic techniques.[1−4] As a solution-processed photovoltaic technique, quantum-dot-sensitized solar cells (QDSSCs) have attracted much attention due to the inherent characteristics of semiconductor quantum dots.[5−11] The quantum confinement effect makes the band gap of quantum dots tunable to match solar spectrum absorption. The high extinction coefficient of quantum dots promises a higher light absorbing efficiency compared with organic dyes in traditional DSCs.[12−16] Moreover, multiple exciton generation and hot carrier collection minimizes the thermalization loss, enabling QDSSCs to break through the theoretical PCE of 31% for single-junction solar cells.[17] An over 6% power conversion efficiency has been achieved on QDSSCs by either using alloyed quantum dot $CdSe_xTe_{1-x}$ or designing ZnSe/CdSe/ZnSe complex quantum dots with a quasi-quantum well structure as new sensitizers to enlarge the electron diffusion length and thus reduce recombination.[18−21]

Except for the optimization of photoanodes, seeking more active and stable catalysts as efficient counter electrodes (CEs) to efficiently reduce S_n^{2-} to nS^{2-} is also highly essential and effective to boost PCE of QDSSCs.[22−25] Nowadays, the copper foil based Cu_2S CE still functions best by greatly reducing the charge transfer resistance at solid/liquid interface (R_{ct2}) to the level of that at solid/solid interface (R_{ct1}) and the intrinsic sheet resistance (R_h) of the CE, which makes both R_{ct1} and R_h become important components in series resistance.[26,27] However, Cu/Cu_2S CEs have issues like mechanical instability and uncertainty due to the reaction of copper and electrolyte. Little attention has been focused on reducing R_{ct1} and R_h in developing new CEs for QDSSCs in previous reports.[26,28] Therefore, an ITO@Cu_2S core−shell nanowire array CE with high quality tunnel junctions has been designed and fabricated in our group, which demonstrated an impressively small R_h and R_{ct2} with no obvious R_{ct1}.[29] This type of CE has several advantages over classic Cu/Cu_2S CEs: (1) ITO nanowire directly grown on FTO or ITO substrate as a substitute for copper foil eliminates the issues of mechanical instability and reaction of copper and electrolyte, and is more practical for actual application in terms of cost and module production,[30] (2) conductive ITO cores facilitate charge transport by shortening transport pathway,[31−33] and (3) the three-dimen-

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sional nanowire array provides more active catalytic sites and easy accessibility for electrolyte.[34−36] Given that the catalytic activity of CE should be proportional to the number of catalytic sites and the interface between ITO and Cu_2S could affect the charge transport and chemical stability of Cu_2S shell on ITO core in electrolyte, several types of ITO@Cu_2S core−shell nanowire arrays with different morphologies, coverage of Cu_2S and interfaces of ITO/Cu_2S were herein fabricated by different methods to investigate these effects. It was found that the successive ionic layer adsorption and reaction (SILAR) method produced a full coverage of Cu_2S nanocrystals on ITO nanowire cores as well as separate Cu_2S nanocrystal aggregates of micrometer size on top of nanowire arrays. Physical vapor deposition via the magnetron sputtering (PVD) method deposited a homogeneous Cu_2S shell with a smooth surface on ITO nanowire cores, but the resulted Cu_2S shell had very poor chemical stability in electrolyte, probably due to inferior interface with ITO. The improved cation exchange method could easily grow a uniform Cu_2S nanocrystal shell on ITO with a good interface, leading to fast charge transport and a higher short-circuit current density as well as high chemical stability. After the optimization of the thickness of the Cu_2S shell, the power conversion efficiency of QDSSCs with the ITO@Cu_2S CE fabricated by this method increased by 16.5% compared to that with the classic Cu/Cu_2S CE, indicating its promising potential as its substitute for QDSSCs.

RESULT AND DISCUSSION

Four types of ITO@Cu_2S core−shell nanowire arrays were fabricated by different methods, including the successive ionic layer adsorption and reaction method (SILAR), physical vapor deposition (PVD), the traditional cation exchange method (EX1), and the improved cation exchange method (EX2). Details for the fabrication are presented in the Experimental Section. Figure 1a−e shows typical high-magnification scanning electron microscopy (SEM) images of pure ITO and ITO@Cu_2S nanowire arrays prepared with these different methods. Pure ITO nanowires display the smooth side surfaces and faceted shape with a diameter in a range of around 100−120 nm (Figure 1a). In the case of the ITO@Cu_2S nanowires synthesized via the EX1 method (Figure 1b), Cu_2S nanocrystals in a diameter of about 20 nm distributed discretely on the ITO nanowire, leaving an appreciable amount of ITO surface uncovered. The SILAR method is frequently used to load quantum dots on mesoporous titania in the fabrication of photoanodes for QDSSCs. As seen in Figure 1c, by using the SILAR route to grow Cu_2S, the ITO nanowire could be effectively covered by Cu_2S nanocrystals with almost no ITO nanowire surface exposed. However, it can also be seen that the growth of Cu_2S was not in a well-defined way. The growth rate varied largely in different positions. Irregular Cu_2S nanocrystals grew on the surface of ITO nanowires or in their interspace. Large aggregates in micrometers could be easily found on the top of ITO@Cu_2S nanowire arrays (see low-magnification SEM image, Figure S1 in the Supporting Information). PVD via magnetron sputtering is a method widely used to form a conformal coating on a variety of materials. In this study, the morphology of ITO@Cu_2S prepared through the PVD route showed a replica of the ITO nanowire core with a very compact and smooth coating (Figure 1d) except that the color of the film turned into dark brown from light blue, which indicated the successful coating of the Cu_2S layer. Lastly, an improved cation exchange method (EX2) was also employed in an attempt to grow a continuous and compact Cu_2S nanocrystal layer coating on the surface of the ITO nanowire cores. The method is referenced to that widely used in thin film solar cells to grow the CdS layer and form a high quality P−N junction with the absorption layer, followed by a cation exchange process to convert CdS into a Cu_2S shell. As shown in Figure 1e, a well-defined ITO@Cu_2S nanowire array with a continuous Cu_2S nanocrystal shell was prepared with the EX2 method. The diameter of the nanowires clearly increased from around 100−120 nm for ITO nanowires to around 250−300 nm for core−shell nanowires. Unlike ITO@Cu_2S prepared via the EX1 method, the entire surface of ITO nanowires was covered with polycrystalline nanocrystals. Figure 1f presents a typical transmission electron microscopy (TEM) image of this type of ITO@Cu_2S nanowire. The clear contrast difference indicates that the nanowire has a core−shell structure. The shell thickness in this case is around 80 nm. It can be also seen that the shell is composed of a continuous layer of polycrystalline nanocrystals with rough surface rather than smooth compact layer like PVD sample, which will provide a larger surface area and thus more catalytic sites when it was used as a CE for QDSSCs.

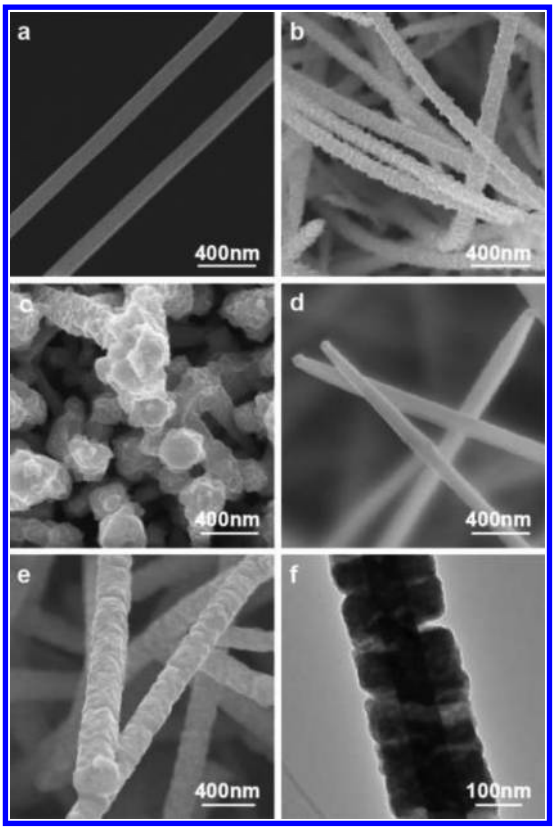

Figure 1. (a−e) Typical SEM images of ITO and ITO@Cu_2S nanowire arrays prepared with different methods: (a) ITO nanowires, (b) EX1-ITO@Cu_2S, (c) SILAR-ITO@Cu_2S, (d) PVD-ITO@Cu_2S, and (e) EX2-ITO@Cu_2S. (f) TEM image of EX2-ITO@Cu_2S.

To confirm the successful growth of Cu_2S and reveal its crystalline structure, X-ray diffraction (XRD) experiments were carried out on all four samples. Figure 2 shows the typical XRD patterns of the ITO nanowire (black line) and four types of ITO@Cu_2S nanowires prepared with different methods. The diffraction peaks of ITO nanowire arrays can be well indexed to cubic In_2O_3 (JCPDS Card No. 06-0416), except for three peaks marked as stars at 26.6°, 51.8°, and 65.9°, which can be

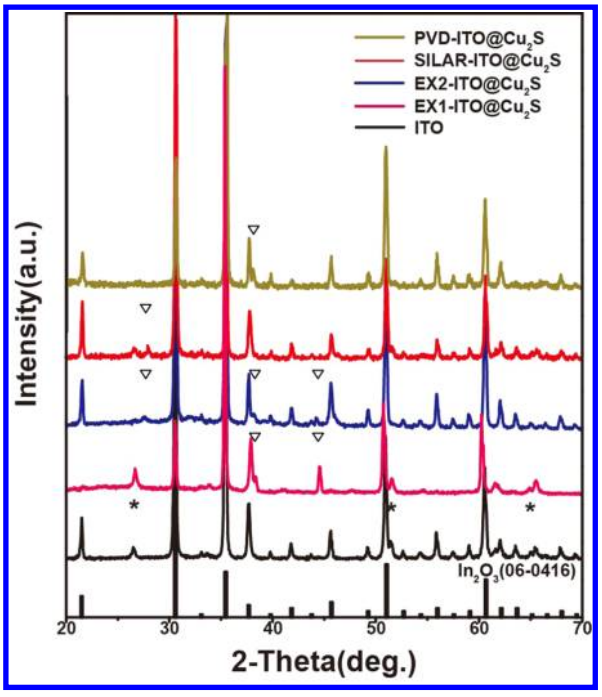

Figure 2. XRD patterns of reference In_2O_3 (JCPDS Card No. 06-0416), ITO (black) and ITO@Cu_2S nanowire arrays prepared with different methods. The peaks marked as stars can be attributed to SnO_2 (JCPDS Card No. 41-1445). The peaks marked as hollow inverted triangles can be ascribed to low-chalcocite Cu_2S (JCPDS Card No. 33-0490).

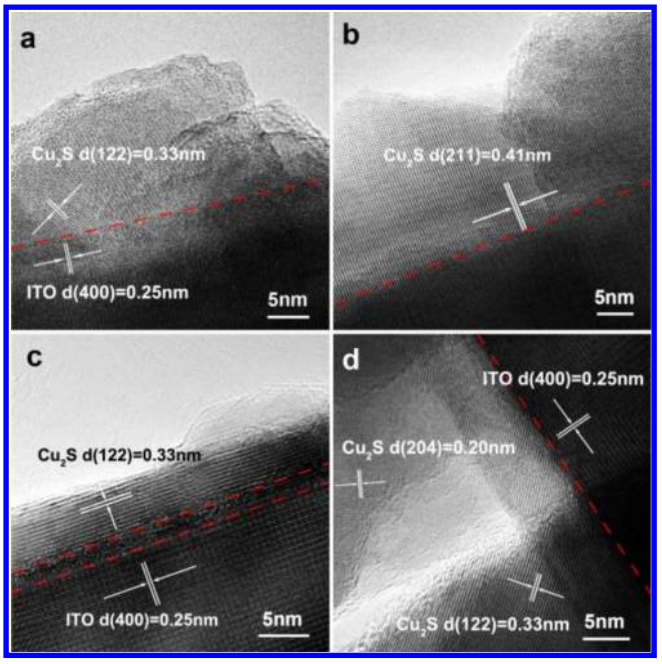

Figure 3. Typical high-resolution TEM images of ITO and Cu_2S interface in different ITO@Cu_2S nanowire: (a) EX1, (b) SILAR, (c) PVD, and (d) EX2. The red dash line in each panel marks the interface.

attributed to the diffraction on the (110), (211), and (301) crystallographic planes of SnO_2 (JCPDS Card No. 41-1445). After the fabrication of Cu_2S through different methods, three more peaks (marked as hollow inverted triangles) at 27.6°, 38.5°, and 44.8° appear, which can be ascribed to the diffraction from the (122), (240) and (204) crystallographic planes of low-chalcocite Cu_2S. A small difference can be found in XRD patterns of different types of ITO@Cu_2S nanowires. Relatively strong diffraction peaks from the (240) and (204) crystallographic planes of Cu_2S emerged in ITO@Cu_2S prepared by the EX1 method, whereas diffraction from (122) planes for the SILAR sample, and (240) planes for the PVD sample were enhanced. All these three diffraction peaks can be distinguished in the EX2 sample. These results confirm that the low-chalcocite Cu_2S formed in all four samples but the crystallographic orientation of Cu_2S nanocrystals might be different in each sample.

High-resolution transmission electron microscopy (HRTEM) was further used to reveal the crystallographic orientation of Cu_2S nanocrystals and investigate the interfaces between ITO and Cu_2S in each case. As shown in Figure 3, clear crystal lattice fringes in the whole imaging region demonstrate that ITO@Cu_2S nanowires prepared by all four synthetic methods were well crystallized. The lattice fringe distance of 0.33 nm in shell parts of ITO@Cu_2S prepared by the EX1 (Figure 3a), PVD (Figure 3c), and EX2 methods (Figure 3d) is consistent with the interplanar spacing (122) planes of low-chalcocite Cu_2S, indicating that Cu_2S nanocrystals were coaxially formed on the surface of the ITO nanowire core. In Figure 3a,d, the lattice fringes of the Cu_2S nanocrystal link smoothly with that of the ITO nanowire core (marked with red dashed line), which indicates the Cu_2S nanocrystals prepared with the cation exchange epitaxially grew on the ITO core. In the PVD case, long continuous lattice fringes with few defects can be observed in the shell part, suggesting the single-crystalline-like Cu_2S shell can be deposited via the PVD route. However, a disordered layer between lattice fringes of ITO and Cu_2S was always found in this case (marked with two red dashed lines in Figure 3c), which means that a defect layer existed between the ITO core and the Cu_2S shell. The existence of this defect layer would be responsible for the chemical instability of this type of ITO@Cu_2S in the electrolyte as mentioned hereinafter. Moreover, continuous lattice fringes of a large size were found in the shell part of the SILAR sample (Figure 3b). No clear interface could be resolved between ITO and Cu_2S along the whole nanowire. This could be probably due to the formation of a thick shell and larger crystal grains. The interplanar spacing of 0.41 nm corresponds to the (211) crystallographic planes of Cu_2S.

Furthermore, the elemental mapping is a powerful technique to characterize the morphology and composition of nanowires with a core−shell structure. Figure 4 shows, as an example, typical results of elemental mapping for a single ITO@Cu_2S nanowire prepared with the improved cation exchange method. Referenced to the morphology shown in low-magnification TEM image (Figure 4a), it can be clearly seen that the elements In (blue) and Sn (yellow) were detected only in the core part, whereas a large amount of Cu (red) was distributed in the whole region of the nanowire. The intensity of the Cu signal in the outer layer was slightly stronger than that in the central part. These results unambiguously corroborated the fact that the Cu_2S layer coaxially grew on the ITO nanowire core. It should be noted that a nickel grid instead of a copper grid was used for sample preparation, to preclude the signal from the TEM grid and get an accurate result in the elemental mapping experiment.

To evaluate the role of the interface engineering of ITO@Cu_2S nanowire array CEs in enhancing the performance of

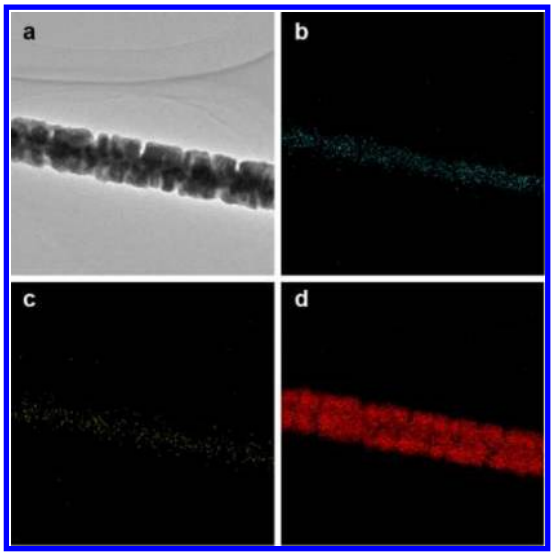

Figure 4. Morphology and of elemental mapping images of EX2-ITO@Cu_2S nanowire: (a) morphology, (b) In, (c) Sn, and (d) Cu.

QDSSCs, we first investigated the influence of annealing on the interface of ITO and Cu_2S and the device performance. Figure S2 (Supporting Information) shows typical TEM images of ITO@Cu_2S nanowire arrays prepared without or with the annealing process at 300 °C after the formation of the Cu_2S shell, with the EX1 method as an example. It is clearly seen that the lattice fringes of Cu_2S nanocrystals before annealing are more disordered than those after annealing. Many more defects were found in the former, while the clearer and more continuous lattice fringes emerged in Cu_2S nanocrystals after annealing, and the interface of ITO and Cu_2S had much less defects in the latter. These results indicate that the crystallinity of Cu_2S nanocrystals and the interface quality of ITO and Cu_2S were much improved by the annealing process. The QDSSCs were further fabricated by using ITO@Cu_2S nanowire arrays without or with the annealing process as CEs. As shown in Figure S3 (Supporting Information), PV−IV measurement revealed that both voltage of open circuit (V_{oc}) and short circuit current density (J_{sc}) of QDSSCs were enhanced by using the annealed CE and thus the device PCE was increased by 21.0% (Table S1, Supporting Information). Therefore, the above-mentioned four types of ITO@Cu_2S nanowire arrays prepared with the EX1, SILAR, PVD, and EX2 methods were annealed before TEM characterization and use as counter electrodes to fabricate QDSSCs. Moreover, the widely used brass based Cu/Cu_2S CE was also compared as a control CE to evaluate the performance of the ITO@Cu_2S nanowire arrays reported here.

Photocurrent−voltage (J−V) curves of all QDSSCs are presented in Figure 5a, and the corresponding data are listed in Table 1. The statistical analysis based on the data measured on five cells for each type of counter electrodes is shown in Figure S4 (Supporting Information). the PVD-ITO@Cu_2S device

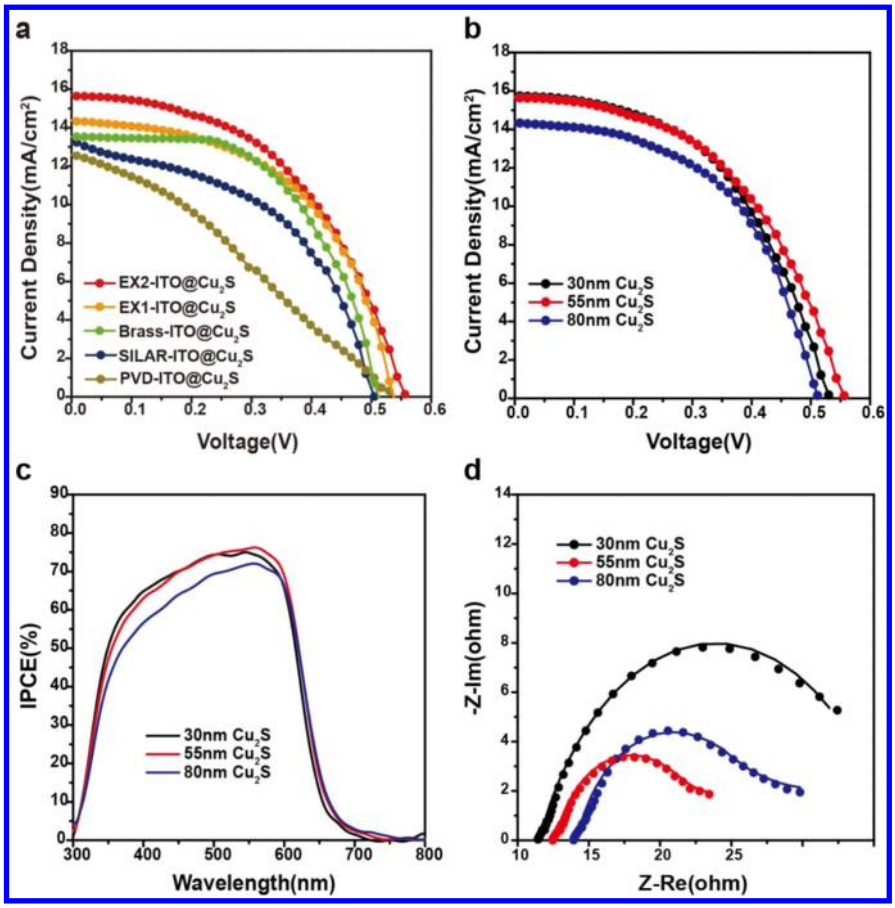

Figure 5. a) Photocurrent−voltage (J−V) curves of QDSSCs with different ITO@Cu_2S CEs. (b) J−V curves and (c) IPCE spectra of QDSSCs fabricated by EX2-ITO@Cu_2S CEs with different Cu_2S shell thicknesses. (d) Nyquist plots from EIS measurements on EX2-ITO@Cu_2S CEs with three thickness of Cu_2S. The dots and the lines are the experimental data and the fitted curves, respectively.

Table 1. Photovoltaic Parameters of QDSSCs with Different CEs

counter electrodes	V_{oc} (V)	J_{sc} (mA cm^{-2})	FF (%)	η (%)
EX1-ITO@Cu_2S	0.540	14.31	52.48	4.06
brass-Cu_2S	0.513	13.54	57.37	3.89
SILAR	0.506	13.34	48.05	3.24
PVD	0.535	12.59	31.67	2.14
EX2-ITO@Cu_2S	0.560	15.55	52.02	4.53

showed the worst performance with the lowest fill factor (FF) of only 31.67% and the lowest J_{sc}, which could be ascribed to the worst interface of ITO and Cu_2S (Figure 3c) and the relatively small surface area of Cu_2S catalysts in view of the morphology with smooth surfaces (Figure 1d). Actually, it should be noted that the dark brown color of the PVD-ITO@Cu_2S CE usually changed to light blue after measurement, implying that the Cu_2S layer partially peeled off from the ITO nanowire during the testing process. This phenomenon could be occasionally observed for the brass-Cu_2S CE, which was due to that Cu_2S on brass lacks chemical stability in a multisulfide electrolyte upon work.

The SILAR-ITO@Cu_2S device showed improved performance better than the PVD-ITO@Cu_2S device but still inferior to the brass-Cu_2S device. The possible reasons are that the SILAR-ITO@Cu_2S had a better interface of ITO and Cu_2S and larger surface area of Cu_2S compared to PVD-ITO@Cu_2S, but the nonuniform growth and inevitable agglomeration of Cu_2S nanocrystals might be unfavorable for the charge transfer from the electrolyte to conductive transparent oxide (CTO) and thus degraded the device performance. On the other hand, ITO@Cu_2S CEs prepared via two kinds of cation exchange methods demonstrated better performance compared to the classic brass-Cu_2S CE. Specifically, device PCE with the EX1-ITO@Cu_2S CE and the EX2-ITO@Cu_2S CE increased by 4.4% and 16.5%, respectively, compared to that with brass-Cu_2S CE. Especially, V_{oc} and J_{sc} of EX2-ITO@Cu_2S device enhanced to 0.560 V and 15.55 mA cm^{-2} from 0.513 V and 13.54 mA cm^{-2} for the brass-Cu_2S device, respectively. This improvement could be attributed to the high-quality interface between ITO and Cu_2S favorable for electron transfer, as well as the three-dimensional structure of nanowire arrays ~10 μm long, which benefits mass transfer and more efficient light scattering in the former. In a comparison of the two cation exchange methods, the EX2-ITO@Cu_2S CE achieved an apparent enhanced performance (11.6% increase in PCE). This could be ascribed to much higher coverage of Cu_2S nanocrystals on ITO, which provided more active catalytic sites. It should be noted that the fill factor of the device with the EX2-ITO@Cu_2S CE was not enhanced compared to that with the EX1-ITO@Cu_2S CE. The reason is that the fill factor is usually related to the series resistance and shunt resistance of a quantum-dot-sensitized solar cell. The series resistance is composed of sheet resistance and charge transfer resistance. Although the EX2-ITO@Cu_2S CE exhibited a smaller charge transfer resistance (1.72 vs 2.64 Ω cm^{-2}) thanks to the more active catalytic sites, it had larger sheet resistance (6.32 vs 4.66 Ω) because it had a thicker Cu_2S shell and the electron conductivity of Cu_2S is smaller than that of ITO (the data can be found in Table 2 and ref 29). Taking into account these two factors together, it is reasonable that the device with the EX2-ITO@Cu_2S CE exhibited a fill factor close to that with the EX1-ITO@Cu_2S CE.

Table 2. Photovoltaic Parameters of QDSSCs and Resistances of Dummy Cells Fabricated by EX2-ITO@Cu_2S CEs with Different Cu_2S Thicknesses

thickness of Cu_2S (nm)	V_{oc} (V)	J_{sc} (mA cm^{-2})	FF (%)	η (%)	R_h (Ω)	R_{ct2} (Ω cm^2)
30	0.534	15.76	49.64	4.18	5.71	3.38
55	0.560	15.55	52.02	4.53	6.32	1.72
80	0.514	14.28	53.64	3.94	7.08	2.00

In further experiments, it was interestingly found that the thickness of the Cu_2S shell in EX2-ITO@Cu_2S can be well controlled by tuning the deposition time of the CdS precursor shell, followed by a solution cation exchange. Three thicknesses of around 30, 55, and 80 nm were chosen in this study. TEM observation displayed that all EX2-ITO@Cu_2S nanowires exhibited very similar core−shell nanowire morphologies with a continuous and compact Cu_2S shell but in different thicknesses. The performance of QDSSCs with these three types EX2-ITO@Cu_2S nanowire array as CEs was measured, and the corresponding data are listed in Table 2. The statistical data are shown in Figure S5 (Supporting Information). As shown in the $J-V$ curves (Figure 5b), V_{oc} and FF of the device increased first as the thickness of the Cu_2S shell in the CEs increased from 30 to 55 nm, but decreased when the thickness further increased to 80 nm. As a result, the device with a 55 nm thick Cu_2S shell reached the highest PCE. This is consistent with the results of incident photon-to-electron conversion efficiency (IPCE) measurements (Figure 5c). The IPCE spectra of devices with 30 and 55 nm thick Cu_2S had nearly the same curve shape, whereas those of the device with 80 nm Cu_2S apparently decreased in the whole wavelength range, resulting in a lower J_{sc}. The highest IPCE of 76.2% was achieved at the wavelength of 560 nm for the device with 55 nm thick Cu_2S.

An electrochemical impedance spectroscopy (EIS) experiment was carried out by using symmetrical dummy cells (two each) of CEs to analyze the sheet resistant and charge transfer resistant in the above-mentioned systems. The measurement was operated at zero potential bias with an AC amplitude of 10 mV and a frequency range between 100 mHz and 100 kHz. The corresponding equivalent circuit is shown in Figure S6 (Supporting Information). The constant-phase element (CPE) was used in the equivalent circuit, and the fitting parameters are listed in Table S2 (Supporting Information). As shown in Figure 5d and Table 2, EIS results indicated that no obvious charge transfer resistances at the solid/solid interface (R_{ct1}) were detected in all CEs, suggesting the high-quality interfaces were achieved between ITO and Cu_2S in all cases so that electrons could be efficiently injected from ITO to Cu_2S. All EX2-ITO@Cu_2S CEs with different thicknesses of Cu_2S shells exhibited a relatively small sheet resistance (R_h) and charge transfer resistance at the solid/liquid interface (R_{ct2}) in several ohms. The undetectable R_{ct1} and small R_h could be attributed to the formation of a high-quality tunnel junction between ITO and Cu_2S because both of them are degenerate semiconductors with a high electron conductivity. R_h increased gradually from 5.71 to 7.08 Ω with the increase of Cu_2S thickness from 30 to 80 nm. The thicker the Cu_2S layer, the longer the electron transfer pathway, which results in the slight increase of R_h. The R_{ct2} between Cu_2S and electrolyte decreased first from 3.38 to 2.00 Ω cm^2 when the thickness of the Cu_2S shell increased from 30 to 55 nm, indicating more efficient electron transfer in the latter, probably due to the increase of the amount of Cu_2S

catalytic sites. In general, the performance of a CE is closely related to its series resistance, which consists of R_h, R_{ct1}, and R_{ct2}. It should consider the balance of three components in optimizing a CE. In the above-mentioned three EX2-ITO@Cu_2S CEs, the CE with the 55 nm thick Cu_2S exhibited the best performance as a result of balancing R_h and R_{ct2}.

The stability is considered to be one of the most critical issues that restricts the application of QDSSCs. The widely used brass/Cu_2S counter electrode usually suffered from the issues of copper dissolution and Cu_2S peel off.[26] To demonstrate the stability of the developed EX2-ITO@Cu_2S CEs, the same CE was used to fabricate three QDSSCs with three photoanodes sequentially. After each time, the cell was measured for more than five times to get the average of the parameters, the CE was disassembled, washed with deionized (DI) water to remove any electrolyte residue, and then used to assemble the next cell. The photovoltaic parameters are listed in Table 3. It was interestingly found that three cells exhibited almost the same performance with very similar photovoltaic parameters. SEM observation was further carried out to investigate the morphology change of the CE before and after three times of measurement. The low-magnification SEM images in Figure 6 clearly revealed that the morphology was nearly unchanged after the whole process. These results demonstrated that EX2-ITO@Cu_2S nanowires were quite stable in the multisulfide electrolyte in the system and could be used as stable CEs for long-life QDSSCs.

Table 3. Photovoltaic Parameters of QDSSCs Fabricated with One Same EX2-ITO@Cu_2S CE and Three Different Photoanodes

serial number	V_{oc} (V)	J_{sc} (mA cm^{-2})	FF (%)	η (%)
1	0.544	14.83	53.62	4.33
2	0.554	14.64	54.19	4.40
3	0.558	14.80	53.04	4.38

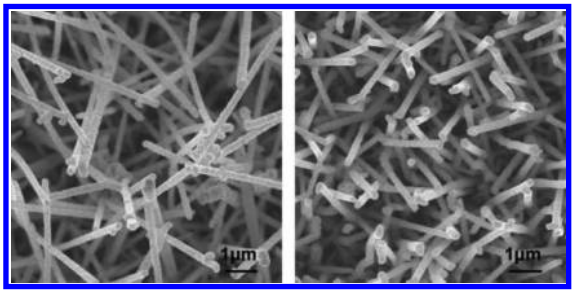

Figure 6. Low-magnification SEM images of the same EX2-ITO@Cu_2S CE: (a) before assembly of QDSSC and (b) after assembly of three QDSSCs with three photoanodes and measurements.

CONCLUSION

In summary, four types of ITO@Cu_2S core–shell nanowire arrays have been fabricated via four synthetic methods, including SILAR, PVD, and two different cation exchange methods, to investigate the influence of morphology, structure, and core–shell interface of ITO@Cu_2S nanowire arrays on their performance as CEs in QDSSCs. It was found that the synthetic methods significantly affected the morphology of Cu_2S shells and the interface between Cu_2S shell and ITO nanowire core. A uniform and continuous Cu_2S nanocrystal shell with a good interface with the ITO core was successfully fabricated on whole surfaces of the ITO nanowire via the improved cation exchange route. With the benefit from the high-quality Cu_2S/ITO interface and three-dimensional core–shell structure of nanowire arrays with a conductive core for facilitating charge transport and a high surface area Cu_2S nanocrystal shell as catalysts, this ITO@Cu_2S nanowire array exhibited impressively small R_h and R_{ct2} as well as undetectable R_{ct1} and thus excellent performance when used as CEs for QDSSCs. By optimizing the thickness of Cu_2S shell, the device PCE with the developed ITO@Cu_2S CE increased by 16.5% compared to that with the classic Cu/Cu_2S CE. In view of no issues of mechanical instability and chemical instability in electrolyte, which Cu/Cu_2S CE usually suffered from, the reported ITO@Cu_2S nanowire array has demonstrated its promising potential as a high-performance CE for QDSSCs.

EXPERIMENTAL SECTION

Synthesis of ITO Nanowire Arrays. FTO glass (14 Ω/□, Nippon Sheet Glass) was used as substrate for ITO nanowire array growth. Before use, it was cleaned by sonicating in water, ethanol, and acetone sequentially, followed by O_2 plasma treatment. A sputtering coater (JFC-1600 Auto Fine Coater, JEOL) was used to sputter Au nanoparticles as catalysts for chemical vapor deposition (CVD) growth. High-purity (99.99%) metallic indium and tin powders were used as sources, in a weight ratio of 10:1, to grow ITO nanowire arrays under an air flow of about 1.5 sccm. The source temperature was 800 °C. Chamber pressure was 30 Pa. After growth, the transparent FTO substrate turned a white-gray color. During the growth, it was found that the average length of the ITO nanowires could be controlled by varying the distance from substrate to the source as well as the growth time. ITO nanowires prepared under exactly the same conditions were used for all the following experiments in this study. The average length was around 10 μm according to SEM observations.

Synthesis of ITO@Cu_2S Nanowire Arrays with SILAR Method. CuCl and Na_2S were used as the Cu^+ and S^{2-} sources for the SILAR process. Typically, ITO nanowire arrays on FTO substrate were successively immersed into 0.1 M CuCl(aq) and 0.1 M Na_2S(aq) for 1 min. Following each immersion, the film was rinsed with DI water for 1 min to remove any excess precursor. This process was repeated for 10 times to achieve a certain amount of Cu_2S loading.

Synthesis of ITO@Cu_2S Nanowire Arrays with the PVD Method. The PVD deposition of Cu_2S on ITO nanowire arrays was conducted on a magnetron sputtering system (PVD75, Kurt J. Lesker, USA) by using a RF power supply of 150 W for 1000 s. A Cu_2S target was used. The pressure was maintained at 3 mTorr. The color of substrate changed to dark brown from light blue after sputtering.

Synthesis of ITO@Cu_2S Nanowire Arrays with Cation Exchange Method EX1. In this procedure, a coaxial CdS shell was first fabricated by chemical bath deposition (CBD). A cation exchange process was then carried out to completely convert the CdS shell to a Cu_2S shell. Typically, ITO nanowire arrays were placed into a solution containing 20 mM $CdCl_2$, 66 mM NH_4Cl, and 140 mM thiourea. The solution temperature was maintained at 25 °C by using a water circulator. After 2 h, the substrate with a yellowish product was washed thoroughly with DI water. A solution cation exchange process was then carried out by immersing the substrate into 0.5 M CuCl(aq) at 50 °C. The light yellow color of the substrate immediately changed to dark brown. Five minutes later, the product was thoroughly washed with DI water, and then dried.

Synthesis of ITO@Cu_2S Nanowire Arrays with Improved Cation Exchange Method EX2. To fabricate ITO@Cu_2S nanowire arrays with a continuous and compact Cu_2S shell, a modified CBD process was used to grow a CdS shell on ITO nanowires. In a typical procedure, ITO nanowire arrays on FTO substrate were put into a flask containing 22 mL of 15 mM $CdSO_4$. NH_4OH(aq) (28 mL NH_4OH in 150 mL of DI water) was then added into the flask. While the solution temperature was maintained at 65 °C, 22 mL of 0.75 M

thiourea was added. After a certain time for designed thickness of CdS, the product was taken out and washed with DI water. A clear color change from white-gray to bright yellow was observed. A solution based cation exchange reaction was subsequently carried out to convert CdS into Cu_2S. In a typical process, the product was immersed into 0.5 M CuCl at 50 °C for 30 min for complete conversion, followed by washing with DI water and drying. The thickness of the Cu_2S shell was controlled by tuning the thickness of the CdS shell, which can be easily adjusted by changing the CBD time. Specifically, 8, 11, and 14 min of CBD can achieve a 30, 55, and 80 nm thick Cu_2S shell, respectively.

Characterization. Field emission scanning electron microscopy (JSM 6701, JEOL, Japan) and transmission electron microscopy (JSM 2100F, JEOL, Japan) were used to characterize the morphologies and compositions of all nanowire arrays. A Rigaku D/max-2500 diffractometer was used to carry out XRD experiments. Electrochemical impedance spectroscopy was carried out and analyzed on a potentiostat (PARSTAT 2273A, Princeton Applied Research).

Preparation of Photoanodes. Photoanodes were prepared by cosensitizing dyesol TiO_2 paste (18NR-T) with CdS/CdSe quantum dots according to literature.[37] In brief, a 9 μm transparent TiO_2 film was coated on FTO substrate, followed by coating a 4 μm TiO_2 scattering layer (200 nm) via a screen printing method. The substrate with the TiO_2 film was treated with $TiCl_4$ and then calcinated. After that, the film was cosensitized with CdS and CdSe quantum dots, and then passivated with ZnS as photoanodes.

Preparation of Counter Electrodes. To improve the interface between the ITO nanowire core and Cu_2S shell, all above-mentioned ITO@Cu_2S nanowire arrays on FTO substrates prepared by different methods were annealed at 300 °C for 30 min within Ar atmosphere, and then directly used as counter electrodes. Brass based Cu_2S counter electrodes were fabricated according to literature.[23]

Preparation of QDSSCs. A series of QDSSCs were fabricated by using the same photoanodes and all above-mentioned ITO@Cu_2S nanowire counter electrodes as well as brass based Cu_2S counter electrodes. The polysulfide electrolyte was prepared by dissolving 1 M S, 1 M Na_2S, and 0.2 M KCl in water/methanol (5:5, v/v). A 3M adhesive tape with a thickness of about 50 μm was used as a spacer to encapsulate electrolyte between the photoanode and counter electrodes.

Photovoltaic Measurements. A solar simulator (450W Model 91150, Newport) with an AM 1.5 spectrum distribution was used as the irradiation source and calibrated against a NREL reference cell to accurately simulate one full-sun intensity (100 mW/cm^2). An IQE-200 measurement system with a motorized 1/8 m monochromator (model 74000, Newport) in DC mode was used for all IPCE tests. A copper mask with a window of 0.16 cm^2 was clipped on the photoanode side of the sandwiched QDSSC to define the active area.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Low-magnification SEM image of SILAR-ITO@Cu_2S nanowire CE, high-resolution TEM images of EX1-ITO@Cu_2S before and after calcination as well as the photocurrent−voltage curves of QDSSCs with the corresponding EX1-ITO@Cu_2S as CEs, statistical analysis on the power conversion efficiencies of QDSSCs with different CEs, statistical analysis on the power conversion efficiencies of QDSSCs with EX2-ITO@Cu_2S CEs in different Cu_2S shell thickness, and equivalent circuits for fitting EIS of CEs. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

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